Mode and a Bit Mode during transfer of the demodulated digital data to said microprocessor, the switching being based upon whether the received digital data is a Packet Mode transmission or a Bit Mode transmission.

8. A data transceiver station according to Claim 7 wherein the transmission line comprises an electrical power line that is part of an electrical power distribution network; and wherein said modem generates information on detection of a voltage level greater than a threshold in a frequency band selected for transmission over the electrical power line.

9. A data transceiver station according to Claim 8 further comprising a zero-crossing circuit for detecting a zero-crossing of the voltage level and for producing a logic signal in response thereto that is input to said modem.

10. A data transceiver station according to Claim 7 wherein said serial interface comprises a receiver section and a transmitter section connected thereto, said transmitter section comprising:

a logic processing circuit for organizing the demodulated digital data into a stream of data structured in packets, and

a multiplexer having a first input for receiving the demodulated digital data and a second input for receiving the stream of data structured in packets, and an output for providing the demodulated digital data or the stream of data structured in packets based upon a selection signal.

11. A data transceiver station according to Claim 7 further comprising an oscillator connected to said modem for providing carrier frequencies thereto.

12. A data transceiver station according to Claim 10 further comprising a memory connected to said logic processing circuit.

13. A data transceiver station according to Claim 10 wherein said logic processing circuit has an input for receiving a first clock signal corresponding to the demodulated digital data; and wherein said logic processing circuit provides a third clock signal comprising a sequence of N pulses having a second clock signal that is a multiple of a frequency of the first clock signal.

14. A data transceiver station according to Claim 10 wherein said multiplexer has a third input for receiving the first clock signal and a fourth input for receiving a fourth clock signal equal to the third clock signal or to the first clock signal based upon whether the selection signal corresponds to the demodulated digital data or the stream of data structured in packets.

15. A data transceiver station according to Claim 10 further comprising a memory connected to said logic processing circuit, wherein said memory comprises:

a first register having a first input for receiving the demodulated digital data and a second input for receiving a first register clock signal, and an output for providing a first data signal; and

a second register having a first input for receiving the demodulated digital data and a second input for receiving a second register clock signal, and an output for providing a second data signal.

16. A data transceiver station according to Claim 15 wherein said logic processing circuit further comprises:

a first counter having an input for receiving the first clock signal and an output for providing a first end-computation signal when N pulses have been counted; and

a second counter having an input for receiving a second clock signal, and an output for providing a second end-computation signal that is enabled by the first end-computation signal and disabled when said second counter counts N pulses of the second clock signal.

17. A data transceiver station according to Claim 15 wherein said logic processing circuit further comprises:

a second multiplexer having a first input for receiving the demodulated digital data and a second input for receiving the third clock signal, and an output for providing the first register clock signal corresponding alternately to the third clock signal and to the first clock signal based upon a switching signal that toggles every N pulses of the first clock signal; and

a third multiplexer having a first input for receiving the demodulated digital data and a second input for receiving the third clock signal, and an output for providing the second register clock signal corresponding alternately to the third clock signal and to the first clock signal based upon the switching signal.

18. A data transceiver station according to Claim 17 wherein said logic processing circuit further comprises a logic AND gate having a first input for receiving the second clock signal and a second input for receiving the second end-computation signal, and an output for providing the third clock signal as periodic sequences of the N pulses when the second clock signal is output at each enablement of the first end-computation signal.

19. A data transceiver station according to Claim 18 wherein said logic processing circuit further comprises a fourth multiplexer having a first input for receiving the first data signal and a second input for receiving the second data signal, and an output for providing a third data signal corresponding to the first data signal or to the second data signal based upon the switching signal.

20. A data transceiver station according to Claim 7 wherein said modem comprises at least one control register for storing the received digital data and for controlling verification thereof.

21. A data transceiver station according to Claim 7 wherein the demodulated digital data is based upon frequency shift keying demodulation.

22. A monolithic integrated multichannel transceiver comprising:

a modem having an input to be connected to an electrical power line of an electrical distribution power network for receiving digital data and an output for providing

a demodulated bit stream in response to the received digital data, said modem for detecting a voltage level in a frequency band selected for transmission over the electrical power line and for providing a logic signal when the voltage level exceeds a threshold;

a serial interface connected to said modem for providing a selection signal based upon the received digital data, said serial interface comprising a receiver section and a transmitter section connected thereto, said transmitter section comprising

a logic processing circuit for organizing the demodulated bit stream into a stream of data structured in packets, and

a multiplexer having a first input for receiving the demodulated bit stream and a second input for receiving the stream of data structured in packets, and an output for providing the demodulated bit stream or the stream of data structured in packets based upon the selection signal; and

a zero-crossing circuit connected to an external coupling circuit connected to the electrical power line for detecting a zero-crossing of the voltage level thereon and for providing an output logic signal to said modem in response to the zero-crossing of the voltage level.

23. A monolithic integrated multichannel transceiver according to Claim 22 wherein the demodulated bit stream corresponds to a Bit Mode transmission and the stream of data structured in packets corresponds to a Packet Mode transmission.

24. A monolithic integrated multichannel transceiver according to Claim 22 wherein said modem comprises at least one control register for storing the received digital data and for controlling verification thereof.

25. A monolithic integrated multichannel transceiver according to Claim 22 further comprising an oscillator connected to said modem for providing carrier frequencies thereto.

26. A monolithic integrated multichannel transceiver according to Claim 22 further comprising a memory connected to said logic processing circuit.

27. A monolithic integrated multichannel transceiver according to Claim 22 further comprising a power interface circuit connected to said modem and for driving the external coupling circuit.

28. A monolithic integrated multichannel transceiver according to Claim 22 wherein said logic processing circuit has an input for receiving a first clock signal corresponding to the demodulated bit stream; and wherein said logic processing circuit provides a third clock signal comprising a sequence of N pulses having a second clock signal that is a multiple of a frequency of the first clock signal.

29. A monolithic integrated multichannel transceiver according to Claim 22 wherein said multiplexer has a third input for receiving the first clock signal and a

fourth input for receiving a fourth clock signal equal to the third clock signal or to the first clock signal based upon whether the selection signal corresponds to the demodulated bit stream or the stream of data structured in packets.

30. A monolithic integrated multichannel transceiver according to Claim 22 further comprising a memory connected to said logic processing circuit, wherein said memory comprises:

a first register having a first input for receiving the demodulated bit stream and a second input for receiving a first register clock signal, and an output for providing a first data signal; and

a second register having a first input for receiving the demodulated bit stream and a second input for receiving a second register clock signal, and an output for providing a second data signal.

31. A monolithic integrated multichannel transceiver according to Claim 30 wherein said logic processing circuit further comprises:

a first counter having an input for receiving the first clock signal and an output for providing a first end-computation signal when N pulses have been counted; and

a second counter having an input for receiving a second clock signal, and an output for providing a second end-computation signal that is enabled by the first end-computation signal and disabled when said second counter counts N pulses of the second clock signal.

32. A monolithic integrated multichannel

transceiver according to Claim 30 wherein said logic processing circuit further comprises:

a second multiplexer having a first input for receiving the demodulated bit stream and a second input for receiving the third clock signal, and an output for providing the first register clock signal corresponding alternately to the third clock signal and to the first clock signal based upon a switching signal that toggles every N pulses of the first clock signal; and

a third multiplexer having a first input for receiving the demodulated bit stream and a second input for receiving the third clock signal, and an output for providing the second register clock signal corresponding alternately to the third clock signal and to the first clock signal based upon the switching signal.

33. A monolithic integrated multichannel transceiver according to Claim 31 wherein said logic processing circuit further comprises a logic AND gate having a first input for receiving the second clock signal and a second input for receiving the second end-computation signal, and an output for providing the third clock signal as periodic sequences of the N pulses when the second clock signal is output at each enablement of the first end-computation signal.

34. A monolithic integrated multichannel transceiver according to Claim 32 wherein said logic processing circuit further comprises a fourth multiplexer having a first input for receiving the first data signal and a second input for receiving the second data signal, and an output for providing a third data signal corresponding to the

first data signal or to the second data signal based upon the switching signal.

35. A method of using a data transceiver station for exchanging digital data over an electrical power line, the data transceiver station comprising a modem connected to the electrical power line, an interface circuit connected to the modem, and a microprocessor connected to the interface circuit, the method comprising:

demodulating the digital data using the modem;

switching the interface circuit between a Packet Mode and a Bit Mode based upon whether the received digital data is a Packet Mode transmission or a Bit Mode transmission; and

transferring the demodulated digital data from the modem to the microprocessor.

36. A method according to Claim 35 wherein demodulating the digital data comprises providing a demodulated bit stream to the serial interface.

37. A method according to Claim 36 further comprising organizing the demodulated bit stream into a stream of data structured in packets.

38. A method according to Claim 37 further comprising providing to a first input of a multiplexer the demodulated bit stream and to a second input of the multiplexer the stream of data structured in packets, and providing at an output of the multiplexer the demodulated bit